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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/118,572
Filing Date: July 17, 1998
Appellant(s): WOOD ET AL.

Terry W. Kramer
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 5/25/2006 appealing from the Office action mailed 12/15/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

Appeal No. 2003-0228

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Rhoades et al. "Real-Time Procedural Textures", Proceedings of the 1992 Symposium in Interactive 3D Graphics, June 1992, pp. 95-100.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. Claims 1-5, 7 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Rhoades et al. ("Real-time procedural textures", June 1992, Proceedings of the 1992 symposium in interactive 3D graphics, page 95-100).

As per claim 1, Rhodes et al., hereinafter Rhodes, disclose an apparatus for texture mapping in a computer graphics system (as illustrated in Figure 1), using a predetermined set of standardized textures ("Procedural textures are implemented via a simple virtual machine. This texture machine comprises an assembly language-like instruction set called T-codes, a set of registers in pixel memory", page 96, 2nd column, line 12-14), the apparatus having an input (since the system is interactive, the processor is inherently having an input in order to receive commands) to receive via a network identifying data identifying one of the set of standardized textures ("Graphics Processors, Renderers, Frame Buffers, and workstation host communicate over a shared 640 Mb/sec ring network", page 96, 15` column, line 20-22; thus, the system forms a network), and

means for processing the data to generate output texels of the identified textures (Figure 1, the Graphics Processor and Renderer process the data), wherein each texture of the standardized set is a procedural texture (where the T-codes are the procedural texture), the identifying data comprises one or a sequence of program commands, the execution of which will result in the generation of a respective procedural texture, with the means for processing data comprising a processor operable

to implement all such input program commands or sequences of input program commands as required to generate the procedural texture of the standardized set (Figure 1, the IGC commands is the instruction streams for the Renderers to rasterize the polygons).

2. As per claim 2, Rhoades demonstrated all the elements as applied to the rejection of independent claim 1, supra, and further discloses having at least one further input for one or more predetermined classes of numerical parameter, with the processor being arranged to generate procedural textures with reference to the or each numerical parameter value received ("This texture machine comprises an assembly language-like instruction set called T-codes, a set of registers in pixel memory, and a set of parameters in the Graphics Processor Memory", page 96, 2nd column, line 13-16, and "the user can explore the parameter space of a procedure continuously in real time", page 98, column 1, line 21-23; thus, the parameters can be changes from input commands).

3. As per claim 3, Rhodes demonstrated all the elements as applied to the rejection of independent claim 1, supra, and further discloses having at least one further input for a scale factor, with the processor being arranged to generate a procedural texture at a resolution determined by a received scale factor ("Examples of operators include add, scale, max, square root, spline, and color lookup", page 96, 2nd column, line 31-32; the parameters are accessible by input commands and scale is listed as one of the parameters).

4. As per claim 4, Rhodes demonstrated all the elements as applied to the rejection of independent claim 1, supra, and further discloses the processor is operable to implement only such input program commands or sequences of input program commands as required to generate those procedural textures of the standardized set ("The texture editor displays the T-code instructions of a selected procedural texture in a text window. The user can position a movable cursor on any literal value in a T-code instruction, and smoothly vary this value via a joystick", page 98, 1st column, line 14-17; since the texture editor can only select procedure textures, it can implement only such input program commands or sequences of input program commands as required to generate those procedural textures of the standardized set.)

5. As per claim 5, Rhoades demonstrated all the elements as applied to the rejection of independent claim 1, supra, and further discloses a cache memory coupled with the processor, with the processor being configured to generate said procedural textures as texture maps within said cache (The Graphics Processor cache the IGC commands resulting from texture interpretation to avoid generating them repeatedly, page 97, 1St column, line 33-35).

6. As per claim 7, Rhoades demonstrated all the elements as applied to the rejection of dependent claim 4, supra, and as for fabricating the apparatus into a single substrate, it is notoriously known in the art (Officially Notice) that a processor of many elements can be fabricated onto a single substrate for the purposes of increasing processing speed and reducing power and cost. See in re Larson, 340 F.2d 965, 144 USPQ 347 (CCPA 1965)

7. As per claim 9, Rhoades demonstrated all the elements as applied to the rejection of independent claim 1, supra, and further discloses a source of three-dimensional polygon data (Figure 1, the Polygon Data in the Graphics Processor), a geometry processor coupled to receive said polygon data and arranged to generate a two-dimensional representation of said polygons (Figure 1, the Graphics Processor), a source of program commands coupled to the input of the texture mapping apparatus and specifying textures to be applied to respective ones of said polygons (Figure 1, the IGC Commands), and rendering means coupled to receive the outputs of the geometry processor and texture mapping apparatus and arranged to generate an output image of said polygons with texture applied (Figure 1, the Renderer).

(10) Response to Argument

Applicant's arguments filed 9/28/2005 have been fully considered but they are not persuasive.

Applicant alleges Rhoades does not teach "using a predetermined set of standardized textures". Applicant alleges Rhodes teaches the procedural texture is user defined, and interactively created and edited. In reply, Examiner considers these "user defined and interactively created and edited" teaching are not in conflict with the claimed limitation. A user defined (and interactively created and edited) texture can be a predetermined texture. On page 98, column 1, line 25-29, Rhodes further teaches "T-code instructions can be added, rearranged, and deleted, producing a new program. Then with a couple of commands, the user can save the updated texture program and reload it into the texture editor for immediate display". The updated texture program

becomes a new predetermined set of standardized textures. And since the texture program can be saved and reloaded, it is further evidence that it is a predetermined texture.

Applicant alleges Rhodes does not teach the apparatus having "an input receive via a network identifying data identifying one of the set of standardized textures". Applicant alleges Rhodes' network is not a data network, such as the Internet/World Wide Web. In reply, since the claim limitation is silent about the nature of "a network", Examiner considers Rhodes' ring network meets the limitation.

Applicant alleges Rhodes does not teach "the identifying date comprises one or a sequence of program commands". In reply, Examiner considers the IGC command instruction stream is a sequence of command and is sent to a Renderer (page 96, column 2, line 20-23). Since a Renderer is a processor, it meets the limitation. Applicant also alleges a SIMD is not a processor. In reply, Examiner considers a SIMD (Single-Instruction Multiple-Data) represents a form of parallel-processor computer architecture, therefore, is a processor.

(11) Related Proceeding(s) Appendix

Copies of the court or Board decision(s) identified in the Related Appeals and Interferences section of this examiner's answer are provided herein.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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